REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 35, 46, 49 and 64 have been amended and new claims 68 and 69 have been added. No new matter has been added. Claims 1-69 are presented for examination. The remarks below refer to the claims as amended herein.

Previously-Filed Drawing Amendment

Applicant amended Figures 5 and 18 of the drawing in a Preliminary Amendment filed February 13, 2004, **but has not received an acknowledgement that the Preliminary Amendment has been entered. Applicant respectfully requests that the Preliminary Amendment be entered and that an acknowledgement of entry be communicated to applicant.** If a copy of the Preliminary Amendment is required, the Examiner is requested to contact the undersigned attorney.

Claim Rejections -- 35 U.S.C. § 103(a)

Claims 1-67 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,154,384 to Nataraj et al. (Nataraj) in view of U.S. Patent No. 6,067,656 to Rusu et al. ("Rusu"). Applicant respectfully disagrees with this reason for rejection.

Claim 1 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, concurrently with the compare operation, whether the selected data word includes an error.

As stated in the Office Action, Nataraj does not disclose an error detection circuit. Rusu discloses an error-detecting system having a CAM array that "determines whether the input data signal matches any tag word stored therein ***without reading the tag words***", and a parity comparator to compare the parity of the input data signal with the parity of a matching tag word (Rusu, col. 4, line 47 - col. 5, line 8, emphasis added). Thus, Rusu discloses an approach for detecting soft errors without reading tag words from the CAM array. Rusu does not disclose or suggest an error detection coupled, via bit lines or any other structure, to receive a data word from one of the rows of CAM cells and to determine whether the selected data word includes an error. Accordingly, even if Nataraj and Rusu could be combined in the manner proposed in the

Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 1 obvious. Because claims 2-15 depend from and further limit claim 1, claims 2-15 also would not have been obvious in view of the proposed combination.

Claim 16 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from a selected one of the rows of CAM cells and a corresponding validity value, the error detection circuit including a first circuit to determine whether the selected data word includes an error, and a second circuit, responsive to an error indication from the first circuit, to output an error signal if the selected data word is determined to include an error, the second circuit including an input to receive the validity value that corresponds to the selected data word and being adapted to prevent assertion of the error signal if the validity value indicates that the selected data word is not a valid data word.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 16 obvious. Because claims 17-20 depend from and further limit claim 16, applicant submits that claims 17-20 also would not have been obvious in view of the proposed combination.

Claim 21 recites in part:

> an error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 21 obvious. Because claims 22-26 depend from and further limit claim 21, applicant submits that claims 22-26 also would not have been obvious in view of the proposed combination.

Claim 27 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a data word from the selected one of the rows of CAM cells and to determine whether the data word includes an error.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 27 obvious. Because claims 28-34 depend from and further limit claim 27, applicant submits that claims 28-34 also would not have been obvious in view of the proposed combination.

Claim 35 recites in part:

> determining, concurrently with the compare operation, whether a selected data word of the plurality of data words includes an error, wherein said determining includes outputting the selected data word from the CAM array.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 35 obvious. Because claims 36-40 depend from and further limit claim 35, applicant submits that claims 36-40 also would not have been obvious in view of the proposed combination.

Claim 41 recites, in part:

> asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word;

Rusu discloses that "Several parity bits may be employed in combination with an error correction code, such as the well-known Hamming code, to determine which bits of the tag word stored in the associated tag memory location, such as the memory location 108, contain an error" (Rusu, col. 5, lines 21-25). Assuming *arguendo* that such several parity bits constitute a validity value, Rusu does not disclose asserting an error signal if the several parity bits indicate that the

tag word is ***valid***. For at least this reason, applicant submits that Rusu does not disclose or suggest the above recited limitation. Because Nataraj also does not disclose the above recited limitation, applicant submits that, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the proposed combination would still lack the above-recited combination and therefore would not have rendered claim 41 obvious. Because claims 42-45 depend from and further limit claim 41, applicant submits that claims 42-45 also would not have been obvious in view of the proposed combination.

Claim 46 recites, in part:

> receiving, from a CAM device that automatically performs error checking operations at a predetermined sequence of error check addresses, an address of a storage location within the CAM device that contains a corrupted data value

As discussed above, Rusu discloses an error-detecting system having a CAM array to determine whether an input data signal matches a tag word therein and a parity comparator to compare the parity of the input data signal with the parity of a matching tag word (Rusu, col. 4, line 47 - col. 5, line 8). Thus, Rusu discloses checking for soft errors in those tag words that match input data signals. Rusu does not disclose or suggest a CAM device that automatically performs error checking operations at a predetermined sequence of addresses, as in the above-recited limitation of claim 46. Because Nataraj also does not disclose the above recited limitation, applicant submits that, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the proposed combination would still lack the above-recited combination and therefore would not have rendered claim 46 obvious. Because claims 47 and 48 depend from and further limit claim 46, applicant submits that claims 47 and 48 also would not have been obvious in view of the proposed combination.

Claim 49 recites, in part

> a CAM device coupled to the plurality of signal lines, the CAM device including an error checking circuit to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error and to signal the processor via one or more of the plurality of signal lines in response to detecting an error in any one of the

plurality of data values

As discussed above, Rusu discloses checking for soft errors in those tag words that match input data signals. Rusu does not disclose or suggest a CAM device to automatically check, in order according to address, each of a plurality of data values stored within the CAM device for error, as in the above-recited limitation of claim 49. Because Nataraj also does not disclose the above recited limitation, applicant submits that, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the proposed combination would still lack the above-recited combination and therefore would not have rendered claim 49 obvious. Because claims 50-56 depend from and further limit claim 49, applicant submits that claims 50-56 also would not have been obvious in view of the proposed combination.

Claim 57 recites, in part:

detecting means for detecting when a valid one of the data words has an error

Applicant submits that, at least for the reasons given with respect to claim 41, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 57 obvious. Because claims 58-63 depend from and further limit claim 57, applicant submits that claims 58-63 also would not have been obvious in view of the proposed combination.

Claim 64 recites, in part:

means for concurrently (i) determining whether a data word stored in a selected row of the CAM cells has an error, including outputting the data word from the selected row of CAM cells; and (ii) comparing comparand data with the data words

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Rusu could be combined in the manner proposed in the Office Action, the combination would still lack the above-recited limitation and therefore would not have rendered claim 64 obvious. Because claims 65-67 depend from and further limit claim 64, applicant submits that claims 65-67 also would not have been obvious in view of the proposed combination.

New claims

Applicant submits that new claims 68 and 69 also include limitations not disclosed or suggested in the proposed combination of Nataraj and Rusu. For example, claim 68 recites, in part:

> outputting a first instruction to the CAM device in response to the error signal, the first instruction instructing the CAM device to output an address of a storage location that contains the corrupted data value

Conclusion

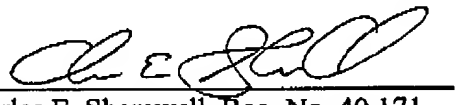
Applicant respectfully submits that claims 1-69 are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 501914 for any fee due in connection with this Amendment.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

Date August 4, 2005



Charles E. Shemwell, Reg. No. 40,171
Tel. 408-236-6645